REMARKS

In response to the Office Action mailed June 7, 2004, Applicant respectfully requests reconsideration.

As a preliminary matter, Applicant notes with appreciation the indication of allowable subject matter in claims 4-6, 12, and 14.

The drawings were objected to because Figures 1-3, according to the Office Action, should be labeled "Prior Art". A proposed drawing correction is enclosed herewith labeling Figures 1-3 as "Prior Art". Review and approval of the proposed drawing correction is respectfully requested.

The Office Action rejected claims 11-14, 21, and 22 under 25 U.S.C. §112, second paragraph, as being indefinite. In particular, the Office Action noted that "sufficient detail interconnections must be recited to adequately describe and constitute the proposed 'carry save adder circuit'".

In response to this rejection, Applicant has amended independent claims 11, 13, 21, and 22 to overcome this rejection. The claims have been amended for clarification only and the amendments do not narrow the scope of the claims.

With respect to claim 14, the dependency has been changed to claim 13. This amendment does not in any way narrow the scope of claim 14.

In view of these corrections to the claims, Applicant believes that the claims satisfy 35 U.S.C. §112 and respectfully requests that the indefiniteness rejection be withdrawn.

Claims 1-3, 11, 15-21, and 23 were rejected under 35 U.S.C. §102(b) as being anticipated by Mou et al.

Claims 1-3, 15-20, and 23 were rejected under 35 U.S.C. §102(e) as being anticipated by Vijayrao et al.

Claims 1-3, 15-20, and 23 were rejected under 35 U.S.C. §102(e) as being anticipated by Eisig et al.

Claims 1-3, 7-10, 13, 15, and 22 were rejected under 35 U.S.C. §102(b) as being anticipated by Griesbach et al.

Applicant respectfully traverses each of these rejections because none of these references, either alone, in combination, or modified as suggested in the Office Action teach or suggest all of the limitations in the independent claims.

Claim 1 recites a carry save adder circuit for reducing the number of inputs to a lower number of outputs, the said carry save adder circuit comprising four carry save adders, said carry save adders being arranged in two layers and wherein said third and four carry save adders each receive at least one output from each of said first and second carry save adders. None of the references teach or suggest the claimed connections among the first, second, third, and fourth carry save adders as claimed in claim 1. Accordingly, claim 1 patentably distinguishes over all of the references and is in allowable condition. Claims 2-10, 15, and 20 depend from claim 1 and are allowable for at least the same reasons.

Claim 11 recites a carry save adder circuit for reducing nine inputs to four outputs, said carry save adder circuit comprising four carry save adders, said carry save adders being arranged in two layers and wherein said third and fourth carry save adders each receive at least one output from each of said first and second carry save adders. None of the references teach or suggest the claimed connections among the first, second, third, and fourth carry save adders as claimed in claim 11. Accordingly, claim 11 patentably distinguishes over all of the references and is in allowable condition. Claims 12-14 depend from claim 11 and are allowable for at least the same reasons.

Claim 13 recites a carry save adder circuit for reducing seven inputs to four outputs, said carry save adder circuit comprising four carry save adder units, said four carry save adders being arranged in two layers and wherein said third and fourth carry save adders each receive at least one output from each of said first and second carry save adders. None of the references teach or suggest the claimed connections among the first, second, third, and fourth carry save adders as claimed in claim 13. Accordingly, claim 13 patentably distinguishes over all of the references and is in allowable condition.

Claim 16 recites an arithmetic unit for processing a plurality of partial products, said unit comprising a plurality of carry save adder circuits each said carry save adder circuit comprising four carry save adders, said four carry save adders being arranged in two layers and wherein said

third and fourth carry save adders each receive at least one output from each of said first and second carry save adders. None of the references teach or suggest the claimed connections among the first, second, third, and fourth carry save adders as claimed in claim 16. Accordingly, claim 16 patentably distinguishes over all of the references and is in allowable condition. Claims 17-19 depend from claim 16 and are allowable for at least the same reasons.

Claim 21 recites an arithmetic unit for processing a plurality of partial products, said unit comprising a plurality of carry save adder circuits, each said carry save adder circuit being arranged to reduce nine inputs to four outputs, said carry save adder circuit comprising four carry save adders, said four carry save adders being arranged in two layers and wherein said third and fourth carry save adders each receive at least one output from each of said first and second carry save adders. None of the references teach or suggest the claimed connections among the first, second, third, and fourth carry save adders as claimed in claim 21. Accordingly, claim 21 patentably distinguishes over all of the references and is in allowable condition.

Claim 22 recites an arithmetic unit for processing a plurality of partial products, said unit comprising a plurality of carry save adder circuits each said carry save adder circuit, being arranged to reduce seven inputs to four outputs, said carry save adder circuit comprising four carry save adder units, said four carry save adders being arranged in two layers and wherein the third and fourth carry save adders each receive at least one output from each of the first and second carry save adders. None of the references teach or suggest the claimed connections among the first, second, third, and fourth carry save adders as claimed in claim 22. Accordingly, claim 22 patentably distinguishes over all of the references and is in allowable condition.

Claim 23 recites a carry save adder circuit for reducing the number of inputs to a lower number of outputs, said carry save adder circuit comprising four carry save adders, said four carry save adders being arranged in two layers and wherein said third and fourth carry save adders each receive at least one output from each of said first and second carry save adders. None of the references teach or suggest the claimed connections among the first, second, third, and fourth carry save adders as claimed in claim 23. Accordingly, claim 23 patentably distinguishes over all of the references and is in allowable condition.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,

Sebastien FERROUSSAT

By: _____

James H. Morris, Reg. No. 34,681
Wolf, Greenfield & Sacks, P.C.
600 Atlantic Avenue
Boston, Massachusetts 02210-2206
Telephone: (617) 646-8000

Docket No.: S1022.80718US00
Date: October 7, 2004
x9/7/04x